



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER OF PATENTS AND TRADEMARKS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
[www.uspto.gov](http://www.uspto.gov)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/830,092	06/27/2001	Kazutaka Shibata	ROH-037	1091

7590 05/12/2003

Rader Fishman & Grauer  
Suite 501  
1233 20th Street NW  
Washington, DC 20036

EXAMINER

MACKEY, TERRENCE M

ART UNIT

PAPER NUMBER

1765

DATE MAILED: 05/12/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)	
	09/830,092	SHIBATA, KAZUTAKA	
	Examiner Terrence Mackey	Art Unit 1765	
-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --			
<b>Period for Reply</b>			
<p>A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.</p> <p>- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.</p> <p>- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.</p> <p>- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.</p> <p>- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).</p> <p>- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).</p>			
<b>Status</b>			
<p>1)<input type="checkbox"/> Responsive to communication(s) filed on _____.</p> <p>2a)<input type="checkbox"/> This action is <b>FINAL</b>.                    2b)<input checked="" type="checkbox"/> This action is non-final.</p> <p>3)<input type="checkbox"/> Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i>, 1935 C.D. 11, 453 O.G. 213.</p>			
<b>Disposition of Claims</b>			
<p>4)<input checked="" type="checkbox"/> Claim(s) <u>1 - 25</u> is/are pending in the application.</p> <p>4a) Of the above claim(s) _____ is/are withdrawn from consideration.</p> <p>5)<input checked="" type="checkbox"/> Claim(s) <u>3 - 16</u> is/are allowed.</p> <p>6)<input checked="" type="checkbox"/> Claim(s) <u>1 - 2, 17 - 25</u> is/are rejected.</p> <p>7)<input type="checkbox"/> Claim(s) _____ is/are objected to.</p> <p>8)<input type="checkbox"/> Claim(s) _____ are subject to restriction and/or election requirement.</p>			
<b>Application Papers</b>			
<p>9)<input type="checkbox"/> The specification is objected to by the Examiner.</p> <p>10)<input checked="" type="checkbox"/> The drawing(s) filed on <u>06/27/01</u> is/are: a)<input type="checkbox"/> accepted or b)<input checked="" type="checkbox"/> objected to by the Examiner.</p> <p style="margin-left: 20px;">Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).</p> <p>11)<input type="checkbox"/> The proposed drawing correction filed on _____ is: a)<input type="checkbox"/> approved b)<input type="checkbox"/> disapproved by the Examiner.</p> <p style="margin-left: 20px;">If approved, corrected drawings are required in reply to this Office action.</p> <p>12)<input type="checkbox"/> The oath or declaration is objected to by the Examiner.</p>			
<b>Priority under 35 U.S.C. §§ 119 and 120</b>			
<p>13)<input checked="" type="checkbox"/> Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).</p> <p>a)<input checked="" type="checkbox"/> All    b)<input type="checkbox"/> Some * c)<input type="checkbox"/> None of:</p> <p style="margin-left: 20px;">1.<input checked="" type="checkbox"/> Certified copies of the priority documents have been received.</p> <p style="margin-left: 20px;">2.<input type="checkbox"/> Certified copies of the priority documents have been received in Application No. _____.</p> <p style="margin-left: 20px;">3.<input type="checkbox"/> Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).</p> <p>* See the attached detailed Office action for a list of the certified copies not received.</p> <p>14)<input type="checkbox"/> Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).</p> <p>a)<input type="checkbox"/> The translation of the foreign language provisional application has been received.</p> <p>15)<input type="checkbox"/> Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.</p>			
<b>Attachment(s)</b>			
<p>1)<input checked="" type="checkbox"/> Notice of References Cited (PTO-892)</p> <p>2)<input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)</p> <p>3)<input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____</p>		<p>4)<input type="checkbox"/> Interview Summary (PTO-413) Paper No(s) _____</p> <p>5)<input type="checkbox"/> Notice of Informal Patent Application (PTO-152)</p> <p>6)<input type="checkbox"/> Other: _____</p>	

## DETAILED ACTION

### ***Drawings***

Figures 19 and 20 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

### ***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

A broad range or limitation together with a narrow range or limitation that falls within the broad range or limitation (in the same claim) is considered indefinite, since the resulting claim does not clearly set forth the metes and bounds of the patent protection desired. Note the explanation given by the Board of Patent Appeals and Interferences in *Ex parte Wu*, 10 USPQ2d 2031, 2033 (Bd. Pat. App. & Inter. 1989), as to where broad language is followed by "such as" and then narrow language. The Board stated that this can render a claim indefinite by raising a question or doubt as to whether the feature introduced by such language is (a) merely exemplary of the remainder of the claim, and therefore not required, or (b) a required feature of the claims. Note also, for example, the decisions of *Ex parte Steigewald*, 131 USPQ 74

(Bd. App. 1961); *Ex parte Hall*, 83 USPQ 38 (Bd. App. 1948); and *Ex parte Hasche*, 86 USPQ 481 (Bd. App. 1949). In the present instance, claim 17 (and dependent claims 18 – 25) recites the broad recitation “chips”, and the claim also recites “chip” which is the narrower statement of the range/limitation.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Michitaka, JP 5-3183. Applicant claims a method for manufacturing a semiconductor device comprising forming projection electrodes on a surface of a semiconductor substrate, forming a protective resin layer on a whole region of the surface of the semiconductor substrate provided with the projection electrodes, a step for removing material by polishing or grinding the backside of the semiconductor substrate, and a step for removing material by polishing or grinding the surface of the semiconductor substrate provided with the projection electrodes to expose the projection electrodes.

Michitaka discloses a method for manufacturing a semiconductor device by forming bump electrodes on the surface of a semiconductor substrate, applying a protective film onto all the surface of the substrate, embedding the bumps therein, grinding the rear side of the semiconductor substrate to thin the substrate, and

removing the protective film through an etch back process to expose the topmost portion of the bump electrodes. The applicant discloses on page 14, lines 11-13, that the protective resin layer may be removed by grinding with a grinder or the like or through another method such as etching. The examiner thus takes the position that polishing of the protective resin layer could be accomplished by an etch back process such as chemical-mechanical polishing.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 2 is rejected under 35 U.S.C. 103(a) as unpatentable over Michitaka in view of Tomonori, JP 5-55278. Michitaka teaches the previously described steps for manufacturing a semiconductor device, however the reference does not teach the step of dividing the semiconductor substrate into individual devices after completing the steps of removing material from the surface and the backside of the semiconductor substrate. Tomonori teaches a semiconductor device manufacture process including a step of dividing a semiconductor substrate following the thinning thereof by a backside

grinding step, the semiconductor substrate having a protective resin film formed on the front surface of the semiconductor substrate in which protrusion electrodes are formed. The protective resin film serves to improve the strength of the semiconductor substrate during the dividing step.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the semiconductor device dicing process as taught by Tomonori in the process of Michitaka to reduce number of process step involved in the forming a plurality of semiconductor devices having a reduced substrate thickness.

#### ***Allowable Subject Matter***

Claims 3 – 16 are allowed. The prior art, either singly or in combination, does not teach a method of manufacturing a semiconductor device comprising steps for forming a surface resin layer on a surface of a semiconductor device, forming a backside resin layer on a backside of the semiconductor substrate, and thinning the semiconductor substrate by removing the backside resin layer and the backside of the semiconductor substrate using a grinding or polishing technique. The prior art, either singly or in combination, does not teach a semiconductor device comprising a solid device, a semiconductor device bonded to the surface of the solid device, projection electrodes for external connection formed on the surface of the solid device, and a protective resin layer for sealing the surface of the solid device with head portions of the projection electrodes thereon exposed.

Art Unit: 1765

It would not have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited prior art so as to arrive at the semiconductor device and above recited manufacturing method as taught by the applicant.

### ***Conclusion***

Remaining references cited of interest to show the state of the art.

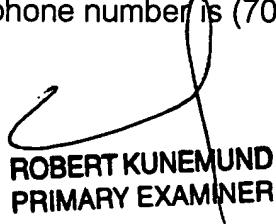
Claims 3 – 16 are allowed.

Papers relating to this application may be submitted to Technology Sector 1700 by facsimile transmission. Papers should be faxed to Crystal Plaza 3, Art Unit 1765, using fax number (703) 305-6357. All Technology Sector 1700 fax machines are available to receive transmissions 24 hrs/day, 7 days/wk. Please note that the faxing of such papers must conform to the Notice published in the Official Gazette, 1096 OG 30, (November 15, 1989).

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Terrence Mackey whose telephone number is (703) 305-5504. The Examiner can normally be reached Monday - Friday from 7:00 AM – 4:30 PM.

If attempts to reach the Examiner by telephone are unsuccessful, the examiner's supervisor, Ben Uteck, can be reached at (703) 308-3836.

Any inquiry of a general nature or relating to the status of this application should be directed to the receptionist whose telephone number is (703) 308-0661



ROBERT KUNEMUND  
PRIMARY EXAMINER